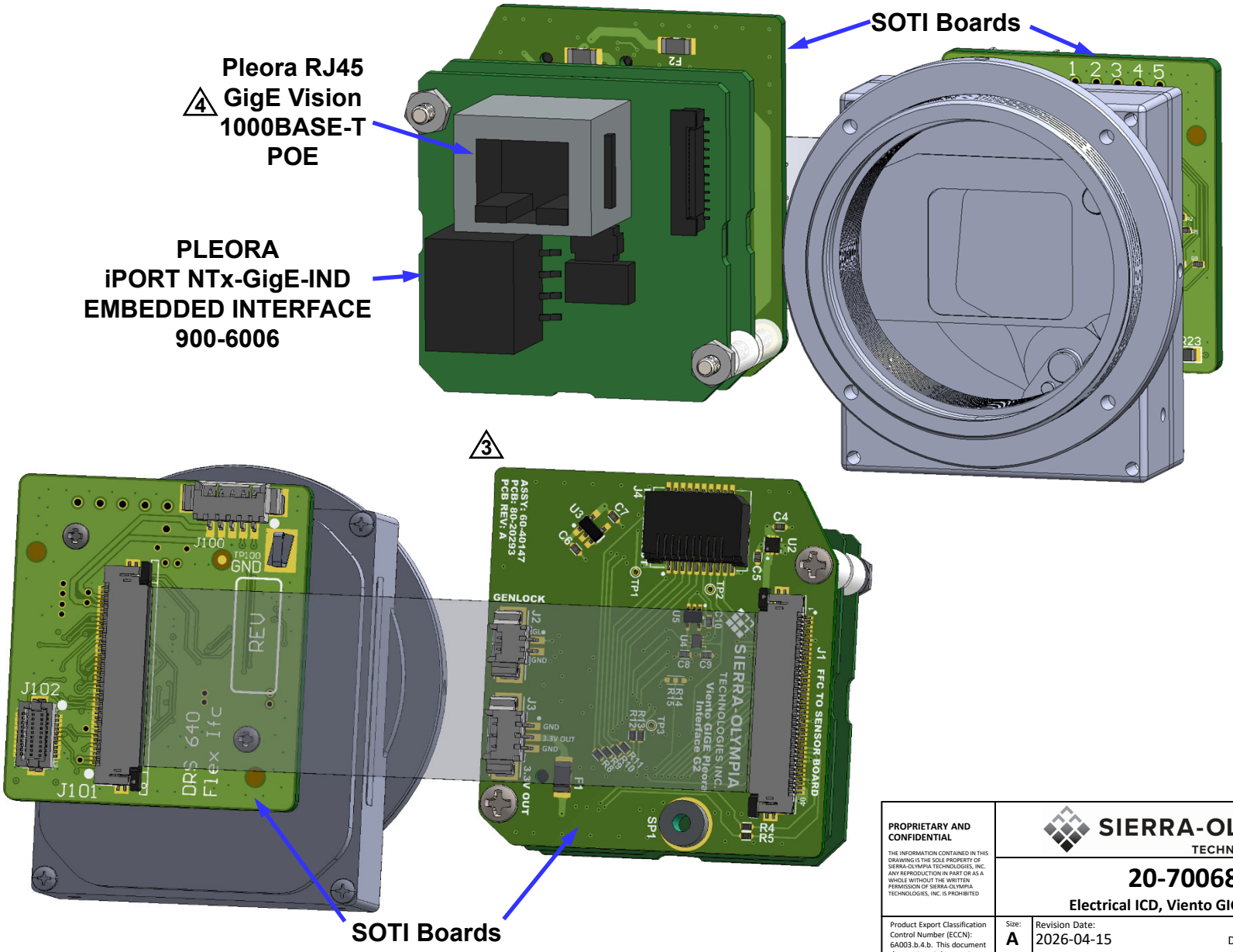
NOTES:

1. LEGEND: ► Position 1 indicator
2. Mating connectors, pinouts, and signal names on Sheets 3-4
3. Image of sensor for reference only. Varies with model.
4. Camera power is provided via Power over Ethernet from the Pleora RJ45 connector.

REVISIONS				
REV	DESCRIPTION	ECO	DATE	Eng.
A	Production Release	1888	2025-07-22	GO
B	Udated PN of Pleora Interface Board	1890	2025-07-28	GO
C	Udated PN for Pleora to Industrial Temp	1974-2	2026-04-15	GO



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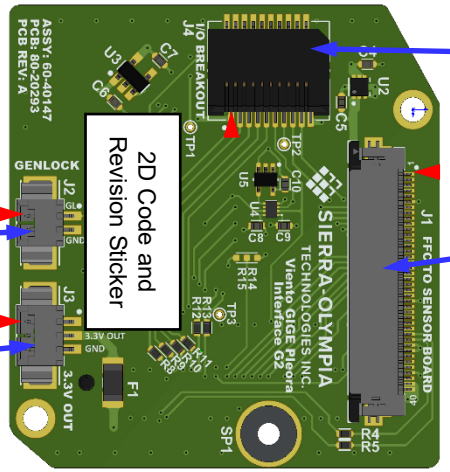
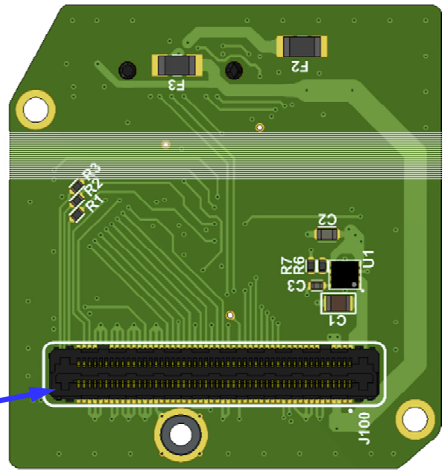
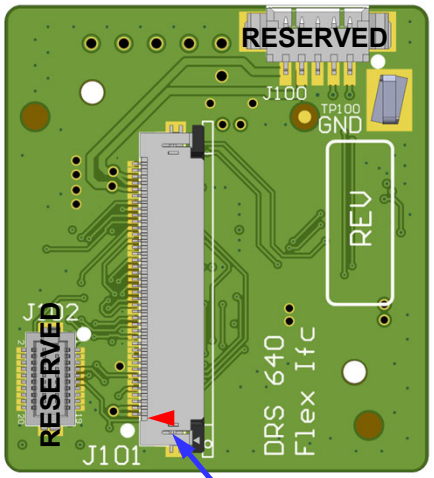




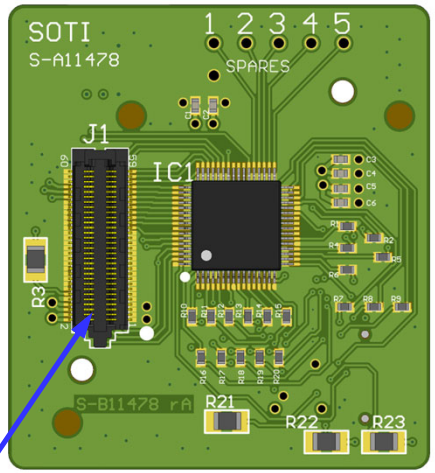
Pleora Interface Board

Sensor Interface Board

Board Top



Board Bottom



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NOTES:

5. Exceeding Max Ratings could cause damage to components.

FFC INTERCONNECT

J1P connects to J101S on the Sensor Interface Board through a 40-pin FFC Cable. The pinout for this interface is intentionally omitted.

Output Connector: Molex 0541044096, Top Contact, Both Boards
Mating cable: 40-position 0.5 mm pitch FFC

J2P - SENSOR GENLOCK

Molex Picoblade 2-position, 1.25 mm pitch
Mating connector housing: Molex 0510210200
Connector terminals: Molex 0500798001 (26-28 AWG)

See DRS ICD for usage of Genlock signal.

Position	Name	Max Rating
1	Genlock I/O ‡	1.8V Logic, -0.3V - 2.25V
2	Ground	-

J3P - AUX 3.3V OUT

Molex Picoblade 3-position, 1.25 mm pitch
Mating connector housing: Molex 0510210300
Connector terminals: Molex 0500798001 (26-28 AWG)

Fuse: Bel Fuse Inc. 0ZCJ0025AF2E

Position	Name	Max Rating
1	GND	250mA Fused Output
2	3.3V Out	
3	GND	

PLEORA INTERFACE BOARD CONNECTORS

J4P - IO BREAKOUT

Connector on board: Amphenol UE75-A20-6000T

This interface breaks out all of the remaining IO available from the Pleora through the GIGE interface. Customers can design their own PCB to fit into this location in order to utilize the IO on this interface.

Usage of these signals though the Pleora GIGE interface can be found in the Pleora User Guide, document number EX001-015-0002.

See Page 4 for PCB Dimension Requirements.

2.5V and 3.3V Fuse: Bel Fuse Inc. 0ZCJ0025AF2E

Position	Name	Description	Max Rating
1	GND	-	-
2	FPGA_GPIO_IN0	Input	2.5V Logic Level IO -0.3V - 3.6V
3	FPGA_GPIO_IN1	Input	
4	FPGA_GPIO_IN2	Input	
5	FPGA_GPIO_IN3	Input	
6	PB0_CTRL_OUT0 ‡	Output	
7	No Connect - TP2	Test Point 2	-
8	PB0_CTRL_OUT2	Output	2.5V Logic -0.3V - 3.6V
9	PB0_CTRL_OUT3	Output	
10	GND	-	-
11	BULK_CLK2	Bulk Interface 2, UART or USRT	2.5V Logic Level IO -0.3V - 3.6V
12	BULK_RXD2		
13	BULK_TXD2		
14	GND	-	-
15	3.3V Out	Power Output	250mA Fused
16	2.5V Out	Power Output	250mA Fused
17	No Connect - TP1	Test Point 1	-
18	BULK_CLK1	Bulk Interface 1, UART, USRT, or I2C	2.5V Logic Level IO -0.3V - 3.6V
19	BULK_RXD1		
20	BULK_TXD1		

‡ SENSOR GENLOCK OPTIONS:

- PB0_CTRL_OUT0 is an output from the Pleora, and is routed to both J4P.6 as an output, and to the FFC as Genlock to the DRS Sensor through a level translator.
- PB0_CTRL_OUT1 is used as a control signal, toggles PB0_CTRL_OUT0 usage.
  - When PB0_CTRL_OUT1 is driven low, PB0_CTRL_OUT0 is connected to sensor's Genlock pin.
    - Genlock on J2P.1 is also driven by PB0_CTRL_OUT0.
    - **This is the DEFAULT if PB0_CTRL_OUT1 is left unprogrammed.**
  - When PB0_CTRL_OUT1 is driven high, PB0_CTRL_OUT0 is disconnected from the sensor's Genlock net.
    - J2P.1 is used to externally connect Genlock to the sensor as an input or an output.

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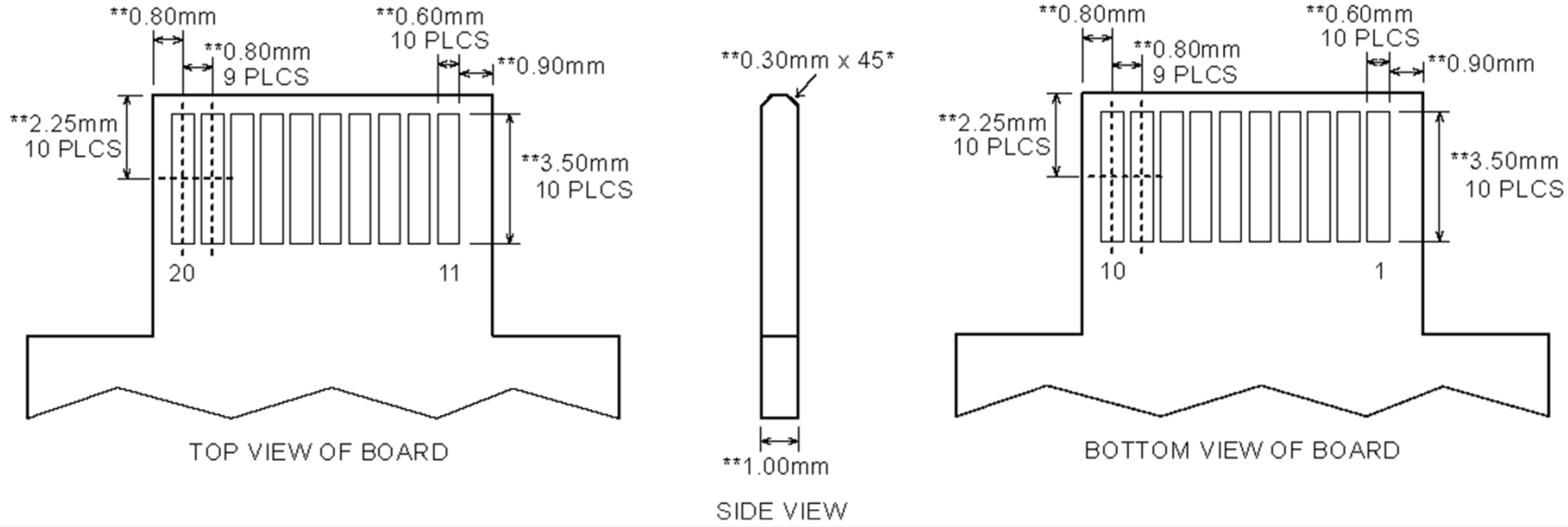
NOTES:

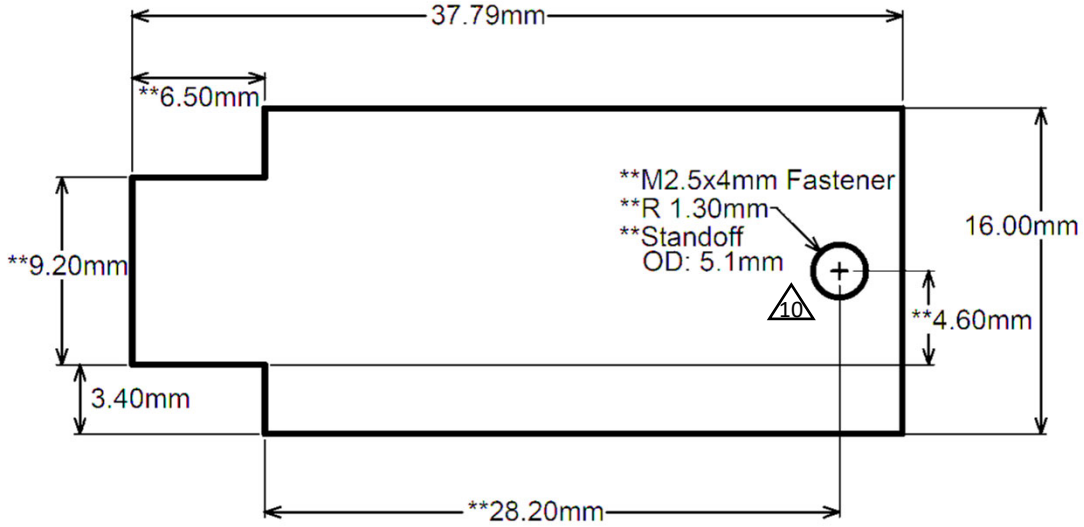
IO BREAKOUT BOARD PCB DIMENSIONS

6. Critical dimensions prefaced by double asterixis **.
7. Tolerances: +/-0.05mm
8. Component Height on bottom side of PCB should not exceed 0.5mm.
9. Component Height on top side of PCB is dependent on user requirements.
10. Use an M2.5x4mm fastener.

J4P Board Edge Detail



Board Outline Detail



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